IN THE SPECIFICATION:

Paragraph beginning at line 17 of page 7 has been amended as follows:

Fig. 1 is a plan view showing a protective transistor according ~~to~~ an embodiment of the present invention;

Paragraph beginning at line 21 of page 7 has been amended as follows:

Fig. 4 is a characteristic graph of a voltage detection circuit; ~~and~~

Paragraph beginning at line 23 of page 7 has been amended as follows:

Fig. 5 shows a structure of ~~Embodiment 1~~ the protective transistor according to the embodiment of the present ~~invention.~~ invention shown in Fig. 1; and

Please add the following new paragraph between lines 1 and 2 of page 8:

Fig. 6 shows another embodiment of the protective transistor according to the present invention.

Paragraph beginning at line 3 of page 8 has been amended as follows:

~~An embodiment~~ Embodiments of the present invention will be described hereinafter. Fig. 1 is a plan view of a protective transistor according to one embodiment of the invention aimed to increase a drain breakdown voltage.

Paragraph beginning at line 16 of page 8 has been amended as follows:

In the structure of the present invention shown in Fig. 1, the drain region 10 is surrounded by the gate electrode 13, which in this embodiment is formed of a polysilicon layer. With this structure, an electrical isolation between the drain region 10 and an element isolation region is kept with a junction diode functioning as a field effect transistor of the gate electrode 13 at an end in a channel length direction. A uniformity of a current path for a noise or static electricity is achieved, thereby making it possible to increase the drain breakdown voltage.

Please insert the following new paragraph between lines 21 and 22 of page 10:

Fig. 6 shows another embodiment of the present invention in which the gate electrode overlaps, rather than surrounds, the drain region 10. By this construction, a

terminal leak current is also suppressed in an operation mode of the semiconductor memory device.